Level-Specific Strategy of KrF Microlithography for 130 nm DRAMs

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1. Introduction

As a minimum linewidth of ULSI patterns approaches the resolution limit in microlithography, the process windows, i.e. depth of focus (DOF) and exposure latitude (EL), are decreasing, and optical proximity effect (OPE) is increasing drastically. There have been a few reports on the extendability of KrF microlithography to 150 nm DRAM. [1][2].

In our previous works [3][4], KrF microlithography was found to be available for 150 nm DRAMs provided the following were applied: a thin resist process technology for enhancing process windows, a simple cell array geometry to avoid complex serif patterns due to large OPE, and lithography design based on lithography simulation.

This paper reports that these technologies enable KrF microlithography to be extended to 130 nm generation in combination with several new technologies. Firstly, focus and dose budget analyses were carried out carefully to estimate their total deviations. Secondly, level specific cell-array patterns and exposure conditions were optimized for obtaining more process windows than the deviations by experiment and simulation. OPE and process proximity effect (PPE) for each level were investigated for core and peripheral circuit patterns.

The key technologies for KrF microlithography, i.e. resolution enhancement technologies (RET) and process proximity correction (PPC), are discussed with a view to realize 130 nm DRAMs.

2. Focus and dose budget analyses

Uncontrollable focus and dose deviations shown in Fig.1 have to be reduced rapidly with RET such as thin resist process [5], off-axis illumination (OAI), and phase-shifting mask (PSM). In view of its small field size, use of scan-type exposure tool can reduce focus error due to wafer flatness and lens aberrations. The variation of critical dimension (CD) of the mask has to be reduced to less than 10 nm (3-sigma) at mask dimension for controlling best exposure dose shift of less than 5 %. In 130 nm generation, the total amount of the focus and dose error can be less than 0.4 um and 9 %, respectively. Therefore, DOF and EL of more than 0.4 um and 9 %, respectively, are necessary for volume production. For storage node (SN) level, more than 14 % EL is necessary because the CD variation results in more than 10 % exposure dose shift. However, 0.4 um DOF and 4 % EL are sufficient for all critical levels of a test vehicle, assuming the area to be guaranteed is small at early stage of development.

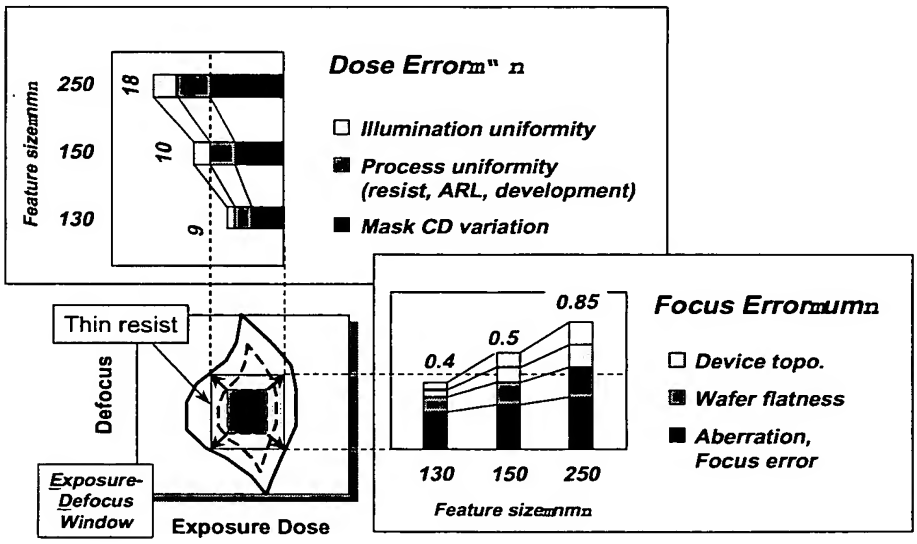

Fig. 1 Focus and dose budget strategy for 130 nm generation

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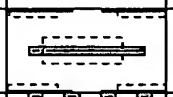
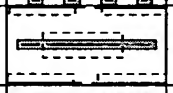
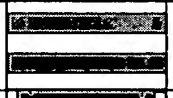
	Mask pattern (solid line) Target pattern (dotted line)	Target CD and tolerances [nm]	Illumination	Resist tone	Exposure latitude [%] (@0.4 um DOF) Target : > 14%(APSM-SN), >9% (Others)			
					Experiment	Simulation		
					KrF+APSM (NA:0.68)	KrF+APSM (NA:0.68)	KrF+APSM (NA:0.73)	ArF+APSM (NA:0.64)
AA		wFVPO} QO xFPRO} PR	Annular	Positive	6.0	1.0	2.6	8.7
				Negative	7.0	6.9	9.3	11.0
GC		wFPRO} PR	Annular	Positive	11.0	11.0	12.0	14.5
PA		wFVWO} QO xFPRO} PR	Annular	Positive	5.0	2.5	4.0	9.2
				Negative	9.0	8.8	9.0	10.4
M0		xFPRO} PR	Annular	Positive	11.0	11.0	12.0	14.5
CB		wFQQO} PR xFQSO} PR	Standard	Positive	11.0	14.9	15.5	21.0
SN		wFSOO} QO xFPXO} PR	Annular	Positive	6.5	8.6	10.6	15.2
			Quadruple	Positive		11.y	14.5	
			Small p	Positive		9.9	Alternating PSM	

Fig. 2 Summary of level specific optimization by simulation and experiment
(Shading boxes represent exposure latitude less than the target)

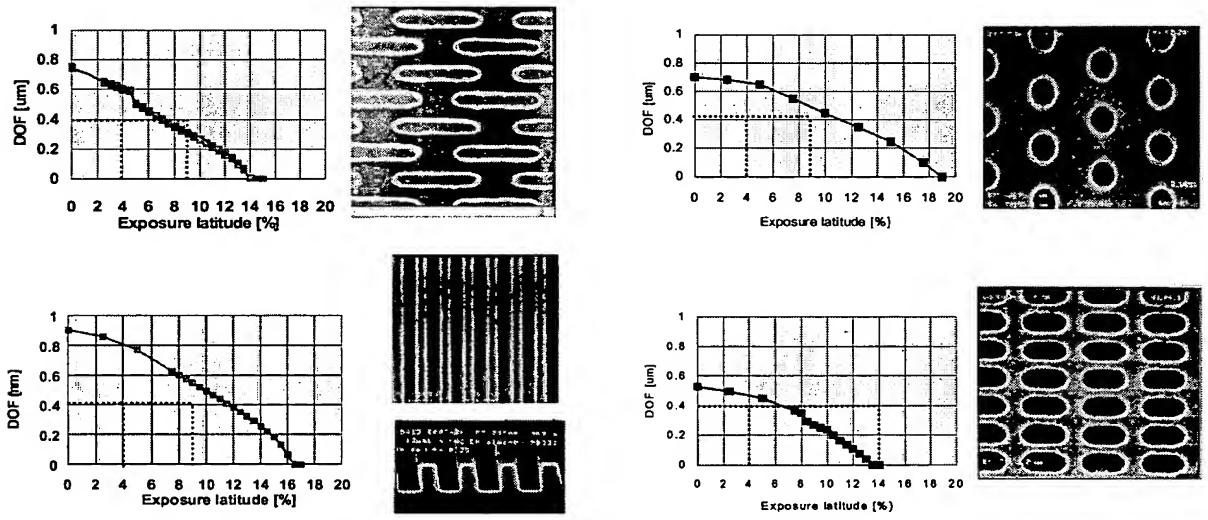


Fig. 3 Experimental result for each level:
(a) AA: negative-resist with 310 nm thickness, (b) GC, M0: positive-resist with 215nm thickness,
(c) CB: positive-resist with 470nm thickness, (d) SN: positive-resist with 450nm thickness
(0.68-NA, 0.75-sigma, 2/3-annular illumination (AA, GC, SN), standard illumination (CB), attenuated PSM)

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3. Level-specific optimization

To achieve the process windows, level-specific cell-array patterns and exposure conditions were optimized by optical lithography simulation taking account of photoresist developing as summarized in Fig. 2. Attenuated PSM (AttPSM) is found to be necessary for all critical levels. For active-area (AA) level and poly-plug-to-AA (PA) level, negative-tone photoresist is especially important for sufficient process windows. The imaging quality for dark field patterns of AA and PA, i.e. DOF, EL, and pattern fidelity, is better than that for bright field imaging. For SN level, quadruple-illumination is essential. For AA, PA, and SN level, higher numerical aperture (NA) lens of around 0.73 is necessary for volume production. Another approach utilizing Alternating PSM (AltPSM) for SN level was also investigated. AltPSM will become a realistic lithographic candidate for SN without core and peripheral circuits if defect inspection and repair technology for the phase shifter is available. Figure 3 shows experimental results of DOF-EL curve for each level. The thickness of the negative-tone photoresist for AA was 310 nm. This result indicates current lithography tool with NA of 0.68 is available for the early stage of device fabrication.

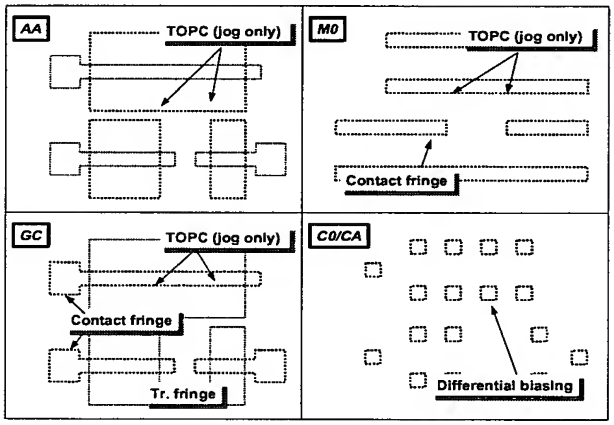

Fig. 4 Level-specific OPC strategy

4. Automated PPC

For all critical levels having core and peripheral circuits, full-chip-level automated PPC technologies were introduced as shown in Fig. 4. All of them were developed in-house. A bucket-rule-based OPC (BOPC) that corrects the edge positions according to "bucket-rule" obtained from the dependence of feature size on distance to the nearest neighbor of test patterns [6] did not have sufficient accuracy for dense line and isolated space patterns. Therefore, AA, gate conductor (GC) level, and first metal (M0) level by damascene process, Toshiba-OPC (TOPC), was adopted because of its high accuracy for dense line and narrow isolated space patterns [7]. TOPC is a hybrid-type tool having rule-based and simulation-based correction scheme as shown in Fig. 5. If one-dimensional context perpendicular to an edge focused on does not exist in the look-up table, the correction engine generates the rule, and corrects the edge position. The rule is stored in the look-up table for future reference. The correction engine consists of an empirical model based on the linear combination of multiple Gaussian

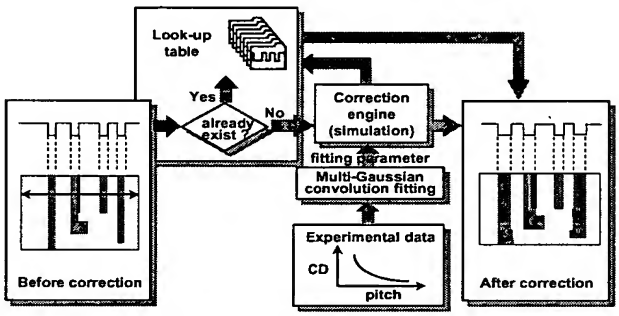

Fig. 5 Correction scheme for TOPC

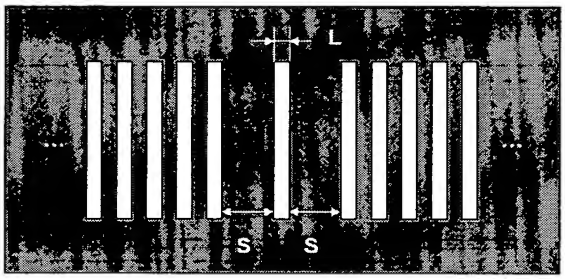

Fig. 6 Patterns for measuring PPE

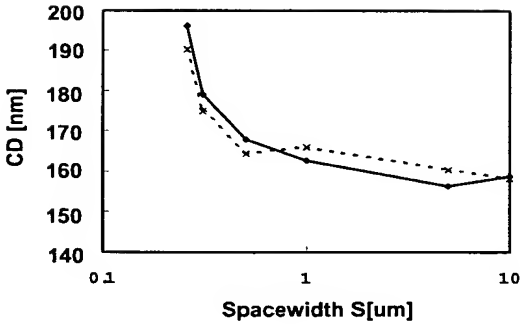

Fig. 7 PPE data and fitting curve by multi-Gaussian function

functions (multi-Gaussian function) so as to fit the experimental PPE data. The experimental PPE data to be fit were obtained by measuring simple one-dimensional patterns shown in Fig. 6 by top-down scanning electron microscopy in advance. The resist and etching process for PPE data acquisition was identical to that for a 130 nm DRAM test vehicle. After statistical processing, the experimental data were fit by the multi-Gaussian function as shown in Fig. 7 [8]. Figure 8 shows the effect of TOPC for M0 level core circuit of the test vehicle. The correction time, excluding look-up table making time, was four hours for M0 level with the data volume of 44.3 MB GDS- format using one 300 MHz SUN UltraSPARC CPU.

5. Conclusions

The viability of KrF microlithography for 130 nm was investigated. It provided adequate DOF and EL with thin resist process, AttPSM, and OAI. The automated PPC for all core and peripheral circuit patterns was introduced. The negative-tone photoresist for AA and PA had a big advantage over the positive tone photoresist. The progress of these ultimate KrF microlithography technologies promises to realize 130 nm DRAMs.

Acknowledgments

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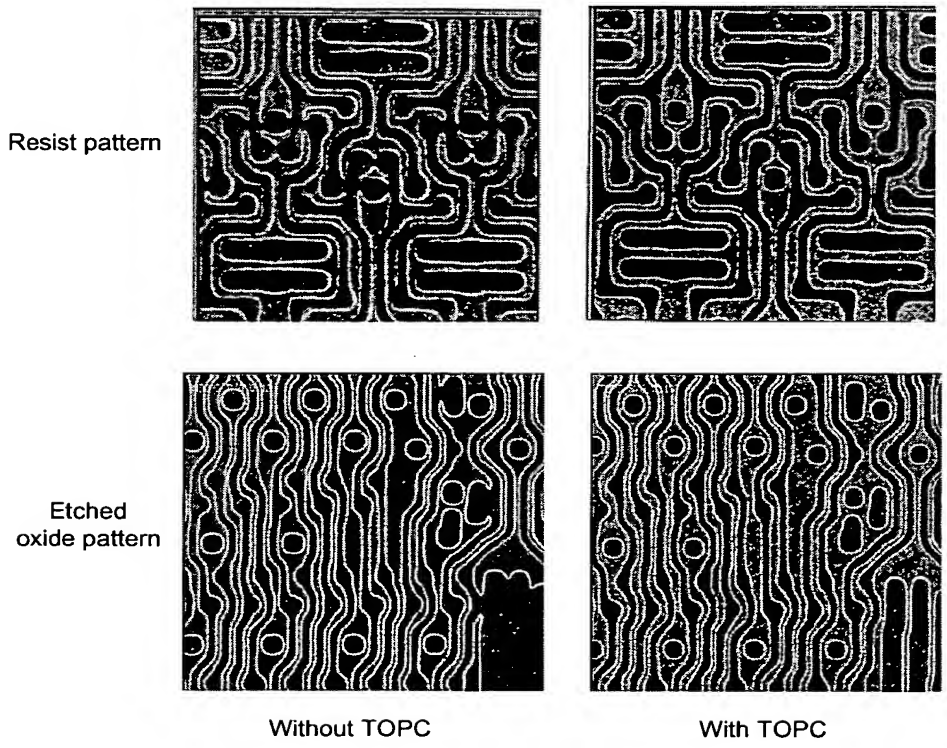

Fig. 8 Effect of TOPC for M0 core circuit patterns with 160 nm feature size